

## REMARKS

This communication is responsive to the Office Action mailed on July 23, 2002. Non-elected claims 16-33 are cancelled. Claims 1-15 have been amended. New claims 34-45 are added. No new subject matter is claimed. Claims 1-15 and 34-45 are pending. Reconsideration in light of the following remarks and amendments is respectfully requested.

### *Election/Restrictions*

As indicated above, non-elected claims 16-33 are cancelled.

### *Specification*

The applicant has found several minor errors in the specification that have been corrected with the amendments noted above.

### *Claim Objections*

Claims 2-14 were amended to change “A circuit” to -- The circuit --. The applicants respectfully submit that the Examiner’s objections to claims 2-14 are now alleviated.

Claim 15 was amended to increase the readability of the claim.

### *Claim Rejections – 35 U.S.C. § 102*

The Examiner rejected claims 1-3 and 7-15 under 35 USC 102(a) as being anticipated by Applicants’ Admitted Prior Art (hereinafter “prior art”).

With regard to claims 1-3, Examiner states that prior art FIG. 5 anticipates the recited elements of independent claim 1. Claim 1 has been amended to recite, in part, “*a read charge control circuit activated only during read operations.*” The addition of this amendment sufficiently distinguishes the prior art, because the read charge control circuit of the prior art is used for read operations as well as write operations (page 3, lines 20-21).

For at least the reason cited above, claims 2, 3, and 7-14 are patentable over FIG. 5 of the prior art.

With regard to independent claim 15, the applicants disagree that prior art FIG. 5 anticipates all claim elements and respectfully submit that the claim is patentable over FIG. 5 for the following reason.

Recited elements of claim 15 include “*a read charge control circuit activated by a read column select line*” and “*a write charge control circuit activated by a write column*

*select line.*" On page 5, lines 1-2, we learn that the read column select line (RCSL) operates during read operations, and the write column select line (WCSL) operates during write operations. FIG. 6 shows that the RCSL and WCSL are separate and distinct.

Unlike the operation of applicants' invention, the CSL of prior art FIG. 5 is not a read column select line that activates a read charge control circuit. The Charge Select Line (CSL) and Read Sense Amplifier (RSA) found in FIG. 5 of the AAPA operate during both read and write operations, which is a stated disadvantage of the AAPA because of increased power consumption (page 3, lines 23-25).

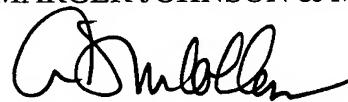
Based on the discussion above, it is apparent that the CSL disclosed in FIG. 5 of AAPA is not equivalent to the recited RCSL of independent claim 15. The applicant respectfully submits that the Examiner's rejection to claim 15 is thereby traversed.

#### ***Claim Rejections – 35 U.S.C. §103***

Claims 4-6 are rejected under 35 USC 103(a) as being unpatentable over prior art FIG. 5, and further in view of prior art FIG. 3. Claims 4-6 are dependent upon claim 1. As explained previously, claim 1 is not anticipated by FIG. 5 of the prior art. Therefore, even if there were motivation to combine prior art FIGS. 3 and 5, all elements of claims 4-6 would not be covered by the combination. The applicants respectfully submit that the Examiner's rejection to claims 4-6 has been overcome for at least the reason above.

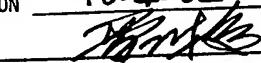
For the foregoing reasons, reconsideration and allowance of claims 1-15 and 34-45 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,  
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**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

**IN THE SPECIFICATION**

Please replace the paragraph beginning page 4, line 28 to 33 with the following:

FIG. 6 shows an embodiment of data path structure having a new high-speed Bit Line Sensing Amplifier (BLSA) for a semiconductor memory device. The BLSA includes a PSA, NSA, RSA, DIOG4, RCSL, WCSL, DIO/DIOB, etc. that operate in a manner as described above. One difference between FIG. 6 and FIG. 5 [in]is the DIOG4. The DIOG4 only has two transistors, N15, N16. This reduces layout area in the memory core. Core refers to a portion of the memory cell arrays, Bit Lines (BLs), BLSA, and Word Line related circuits, etc.

Please replace the paragraph beginning page 6, line 14 to line 23 with the following:

FIG. 12 shows another embodiment where a Mode Register Set (MRS) command or signal is generated in the DRAM right after power-up. The MRS may be programmed after power-up and before normal operation. In addition, the MRS may also be changed during normal operation. The MRS command[.] or signal is applied for initially determining how the DRAM operates. The MRS signal sets CL (CAS Latency), BL (Burst Length), etc., and is a combination of external command signals (CLOCK, CSB, RASB, CASB, WEB) and a plurality of addresses. The CSB signal refers to a chip select signal and the RASB signals refers to a row address strobe signal. The CASB signals refers to a column address strobe signal and the WEB signal refers to a write enable signal. The last character “B” refers to a bar-triggered-enable signal.

**IN THE CLAIMS**

1. (Amended) A circuit, comprising:

a read charge control circuit activated only during read operations by a read signal and an address; and

a write charge control circuit activated by a write signal and the same or a different address, the read charge control circuit and the write charge control circuit both coupled to common data IO lines.

2. (Amended) [A] The circuit according to claim 1 wherein the read charge control circuit is a sense amplifier.

3. (Amended) [A] The circuit according to claim 1 wherein the write charge control circuit transfers charge between the data IO lines and bit lines.

4. (Amended) [A] The circuit according to claim 1 wherein the write charge control circuit includes only two write controlled gates, a first one of the write controlled gates controlling charge of a bit line and a second one of the write controlled gates controlling charge of a complementary bit line.

5. (Amended) [A] The circuit according to claim 4 wherein the first and second write controlled gates are both controlled by a write column select line signal.

6. (Amended) [A] The circuit according to claim 4 wherein the first write controlled gate is coupled directly between the bit line and a data IO line and the second write controlled gate is coupled directly between the complementary bit line and a complementary data IO line.

7. (Amended) [A] The circuit according to claim 1 wherein the read charge control circuit includes a first read controlled gate controlling charge from a bit line to a complementary data IO line and a second read controlled gate controlling charge from a complementary bit line to a data IO line.

8. (Amended) [A] The circuit according to claim 7 wherein the first and second read controlled gates are both controlled by a read column select line signal.

9. (Amend) [A] The circuit according to claim 7 wherein the first read controlled gate is coupled directly between the bit line and the complementary data IO line and the second read controlled gate is coupled directly between the complementary bit line and the data IO line.

10. (Amend) [A] The circuit according to claim 1 including a data output sense amplifier coupled between a data output buffer and the data IO lines.

11. (Amended) [A] The circuit according to claim 10 including load transistors shared between the read charge control circuit and the data output sense amplifier.

12. (Amended) [A] The circuit according to claim 1 wherein the read charge control circuit includes:

a first transistor having a first terminal coupled to a bit line, a second terminal coupled to a complementary data IO line and a third terminal;

a second transistor having a first terminal coupled to a complementary bit line, a second terminal coupled to a data IO line and a third terminal; and

a third transistor having a first terminal coupled to a column select line, a second terminal coupled to the third terminal of the first and second transistor and a third terminal coupled to a first reference voltage.

13. (Amended) [A] The circuit according to claim 12 wherein the write charge control circuit includes:

a first transistor having a first terminal coupled to a write column select line, a second terminal coupled to the complementary bit line and a third terminal coupled to the complementary data IO line; and

a second transistor having a first terminal coupled to the write column select line, a second terminal coupled to the data IO line and a third terminal coupled to the bit line.

14. (Amended) [A] The circuit according to claim 13 including a first load transistor having a first terminal coupled to a second reference voltage, a second terminal coupled to the data IO line and a third terminal coupled to a third reference voltage; and a second load transistor having a first terminal coupled to the second reference voltage, a second terminal coupled to the complementary data IO line and a third terminal coupled to the third reference voltage.

15. (Amended) A circuit, comprising:

a read charge control circuit activated by a read column select line; [and]

a write charge control circuit activated by a write column select line, wherein the read charge control circuit and the write charge control circuit are both coupled to common data IO lines;

a data output sense amplifier; and

load transistors shared by both the read charge control circuit and the data output sense amplifier.

Cancel claims 16-33.

Claims 34-46 are new.